	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	267	(pipelined adj processor).clm.	US-PGPUB; USPAT	2007/06/01 09:23
2	BRS	L2	5670	(power adj2 controller).clm.	US-PGPUB; USPAT	2007/06/01 09:24
3	BRS	L3	51192	model.clm.	US-PGPUB; USPAT	2007/06/01 09:25
4	BRS	L4	38	(maximum adj average adj power).clm.	US-PGPUB; USPAT	2007/06/01 09:26
5	BRS	L5	61	(throttl$3 near3 instruction).clm.	US-PGPUB; USPAT	2007/06/01 09:26
6	BRS	L6	1	1 and 2 and 3 and 4 and 5	US-PGPUB; USPAT	2007/06/01 09:27
7	BRS	L7	37	(average adj2 power adj dissipation).clm.	US-PGPUB; USPAT	2007/06/01 09:29
8	BRS	L8	167	(stall$3 adj2 instruction).clm.	US-PGPUB; USPAT	2007/06/01 09:30
9	BRS	L9	144039	threshold.clm.	US-PGPUB; USPAT	2007/06/01 09:30
10	BRS	L10	101660	register.clm.	US-PGPUB; USPAT	2007/06/01 09:30
11	BRS	L11	2	1 and 7 and 8 and 9 and 10	US-PGPUB; USPAT	2007/06/01 09:33
12	BRS	L12	39	(bleed adj rate).clm.	US-PGPUB; USPAT	2007/06/01 09:34
13	BRS	L13	7	(issue adj weight).clm.	US-PGPUB; USPAT	2007/06/01 09:34
14	BRS	L14	2	1 and 8 and 9 and 10 and 12 and 13	US-PGPUB; USPAT	2007/06/01 09:36